

EC 304 – DIGITAL ELECTRONICS

Teaching Scheme			Examination Scheme							
Lect.	Pract	Total	Theory				Practical			Grand Total
			Int. Assess.	Sem End Marks	Sem End Hrs	Total	Int. Assess.	Sem End	Total	
4	2	6	30	70	3	100	25	25	50	150

1. Binary Systems:

Digital Computer & Systems, Binary Numbers, Number Base conversions, Different Number systems & their relations, Complements, Binary codes, Binary storage & registers.

2. Digital Integrated Circuits:

RTL, DTL circuits, I²L Logic, TTL, ECL, MOS & CMOS circuits & their characteristics, source current & sink current.

3. Boolean Algebra & Logic Gates:

Basic definitions, Axiomatic definition of Boolean Algebra, Basic Theorems & Properties, Boolean functions, Canonical & Standard forms, Logic operations, Digital Logic gates & Logic families.

4. Simplification of Boolean Functions:

Map method, Two, Three, Four, Five & Six variable maps, Products of Sum & Sum of Products simplification, NAND, NOR & Other two level Implementations, Don't care conditions, Tabulation method.

5. Combinational Logic:

Design Procedure, Adders, Subtractors, Code Conversion, Analysis Procedure, Multilevel NAND & NOR circuits, Exclusive-OR & Equivalence functions.

6. Combinational Logic with MSI & LSI:

Binary Parallel Adder, Decimal Adder, Magnitude Comparator, Decoders, Multiplexers, ROMs, PLAs, introduction of PLDs, CPLDs and FPGA..

7. Sequential Logic:

Latch, Flip Flops, difference between latch and flip flop, Triggering of Flip flops, Analysis of clocked sequential circuits, State reduction & assignment, Flip Flop Excitation tables, Design of Sequential circuits, Design of counters, Design using state equations.

8. Registers and Counters:

Registers, Shift registers, Ripple Counters, Synchronous Counters, Memory.

Reference books:

1. Morris Mano, Digital Logic and Computer Design
2. Floyd, Digital Fundamentals
3. Donald D Givone, Digital Principles and Design
4. William Kleitz, Digital Electronics-A Practical Approach
5. R. P. Jain, Digital Electronics
6. Brian Holdsworth, Digital Logic Design